Process Parameters Optimization of 14nm p-Type MOSFET using 2-D Analytical Modeling

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***Abstract*—Simulations of a computer-generated downscaled device at 14nm gate length of p-type MOSFET is conferred in this paper. The device is scaled down from a 32nm transistor which is from the former research. A combination of insulator-conductor that were used includes a high-k material and a metal gate where in this research, Hafnium Dioxide (HfO_2) is used as high-k material and Tungsten Silicide (WSi_2) is used as a metal gate. A 14nm p-type transistor was virtually fabricated using ATHENA module and characterized its performance evaluation using ATLAS module in Virtual Wafer Fabrication (VWF) of Silvaco TCAD Tools. The scaled down device is then optimized through process parameter variability using Taguchi Method. The objective is to find the best combination of fabrication parameter in order to achieve the targeted value of threshold voltage (V_{TH}) and leakage current (I_{OFF}) that are predicted by International Technology Roadmap for Semiconductors (ITRS) 2013. The results show that the ideal value for V_{TH} and I_{OFF} are 0.248635±12.7% V and $5.26x10^{-12}$ A/um respectively and the results were achieved according to the ITRS specification.**

***Index Terms*—14nm p-type MOSFET; High-k Dielectric; Silvaco; Taguchi Method.**

I. INTRODUCTION

The effort in downscale the Complementary Metal Oxide Semiconductor (CMOS) has been pursued continuously following the Moore's Law ever since the early of 1970s. Since then, this road always faces various challenges as the consumers' demands for high speed but low power device. The reduction in transistor size might improve a device performance since many transistors can be compact in a single chip and thus reduce the propagation delay. However, this will cause overheating and increasing in power consumption which leads to a higher leakage current. This is due to the non-linearity of physical and electrical characteristic of the materials in the devices. There are many device performance related problem when the gate length is downsized such as Short-Channel Effect (SCE), Drain Induced Barrier Lowering (DIBL) and Hot Carrier Effect [1]. The SCE arises due to downscaling and affects changes in the electric field at the drain and source area and influence the charge distribution. This scenario will negatively influence the basic characteristics of transistor device and hence will contribute to the complexity in getting a good threshold voltage (V_{TH}) and leakage current (I_{OFF}) value.

Convolution in downscaling has risen the interests in researchers and IC manufacturers. Competing in device progression, many ideas has been proposed such as vertical gate, FinFET and new material such as graphite. A gate length of 12nm and 14nm modified double gate MOSFET which utilized the conventional SiO2/Poly-Si is discussed in [2] and [3] respectively. The performance of 14nm SOI FinFET is demonstrated in [4]. Even though hold a very small gate length, these design proved that the scaling down to 12nm is possible besides a promising performances characteristic.

In this research, a 14nm p-type transistor was scaled down from the former 32nm device which can be seen in [5]. The transistor is simulated through ATHENA module and its electrical characteristic is simulated through ATLAS module. These modules are important in designing and optimizing the process parameter [7]. In this paper, Taguchi method was used to observe the variance and mean effect of process parameters as part of optimization process of threshold voltage and leakage current. Furthermore, Taguchi method is an important element in robust design because it helps to reduce development time and to ensure that the product is in good quality. In recent year, the Taguchi method become one of the greatest tools to improve product and design during research and development process that can produce high quality product at low cost [8]. The aim of this research is to virtually design a 14 nm high-k metal gate transistor with V_{TH} value of 0.2301V and I_{OFF} lower than 100 nA/um which is set by ITRS 2013 specification.

II. METHODOLOGY

A. ATHENA Simulation Recipe

The fabrication process of 14 nm gate length p-type transistor was designed virtually through ATHENA module following previous experiment in [5, 11, 12] except the different number of dopants due to the different size and gate length of the transistor. The summarized fabrication recipe of 14nm device design was shown in Table 1. Figure 1 show the

complete doping profile of the 14 nm $HfO_2/TiSi_2$ transistor. The result of doping concentration determined the electrical characteristic of the device. A good doping concentration will ensure the transistor to work effectively with perfect gate control and low leakage current [9].

Table 1
Fabrication Recipe

Process step	Parameters
Silicon substrate	<100> orientation
Retrograde well implantation	• 200Å oxide screen by 970˚C, 20 min of dry oxygen • 4.55 x $10^{11}cm^{-3}$ Phosphorus • 30 min, 900˚C diffused in nitrogen • 36 min, dry oxygen
STI isolation	• 130Å stress buffer by 900˚C, 25min of dry oxygen • 1500Å Si_3N_4, applying LPCVD • 1.0um photoresist deposition • 15 min annealing at,900 ˚C (X1) and 910 ˚C (X2)
Gate oxide	Diffused dry oxygen for 0.1 min,815 ˚C
Vt adjust implant	• 1.8 x $10^{11}cm^{-3}$ Boron difluoride • 5KeV implant energy,7˚ tilt • 20 min annealing at, 795 ˚C (Y1) and 800 ˚C (Y2)
High-K/Metal gate deposition	• 0.002um HfO_2 • 0.1um $TiSi_2$ • 17 min, 900 ˚C annealing
LDD implantation	• 5.05 x $10^{13}cm^{-3}$ Phosphor • 20˚ tilt
Sidewall spacer deposition	• 0.047um Si_3N_4
S/D implantation	• 9.20 x $10^{12}cm^{-3}$ Boron • 10KeV implant energy • 7˚ tilt
PMD deposition	• 0.3um BPSG • 25 min, 850 ˚C annealing
Metal 1	• 0.04um Aluminium
IMD deposition	• 0.005um BPSG • 15 min, 950 ˚C annealing
Metal 2	• 0.12um Aluminium

B. Taguchi L9 Orthogonal Array Method

The optimizations of a 14nm p-type transistor device were performed using Taguchi L9 method where 36 simulations of three different factors were analyzed at four different noise factors to evaluate the optimum value V_{TH} and I_{OFF}. The parameters that were used in this experiment includes Halo implantation dose, Halo tilting angle, Source Drain implantation and Compensation implantation. Noise factors on the other hands include Sacrificial Oxide Layer Temperature and V_T Adjust Implant Temperature. These parameters were chosen based on its impact to the device performance such that a slight number in dopant changes in any parameters might either deteriorate the device performance or probably enhances it [12]. The value for each level of process parameters and noise factors are listed in Table 2 and Table 3 respectively.

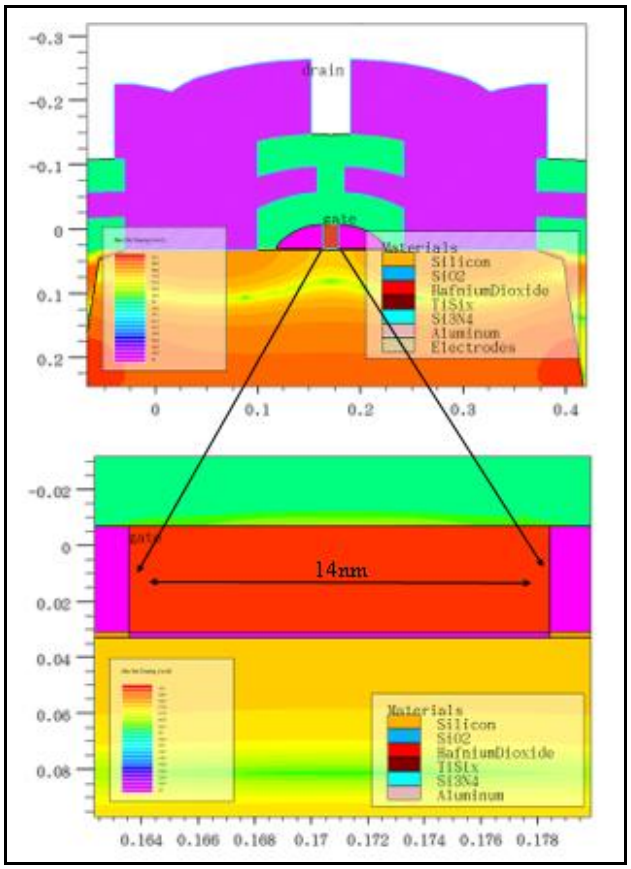

Figure 1: Doping Profile of 14 nm p-Type Transistor

Table 2
Control Factor and Their Level

Process Parameter	Unit	Level 1	Level 2	Level 3
Halo Implantation Dose (A)	atom/cm^3	5.05 x 10^{13}	5.10 x 10^{13}	5.15 x 10^{13}
Halo Tilt Angle (B)	◦	19.7	19.8	19.9
S/D Implantation Dose (C)	atom/cm^3	9.00 x 10^{12}	9.10 x 10^{12}	9.20 x 10^{12}
Compensation Implantation Dose (D)	atom/cm^3	0.4 x 10^{11}	1.1 x 10^{11}	1.8 x 10^{11}

Table 3
Noise Factor and Their Level

Symbol	Noise factor	Unit	L1	L2
X	Sacrificial Oxide Layer Temperature	^{0}C	900	910
Y	V_T Adjust Implantation Temperature	^{0}C	795	800

C. Atlas Overlay Results

The electrical characteristic graphs of p-type transistor were generated by ATLAS module. Figure 2 shows a graph of I_{DS}-V_{DS} at different gate voltage (V_{GS}) and Figure 3 shows the graph of I_{DS}-V_{GS} at different drain voltage (V_{DS}).

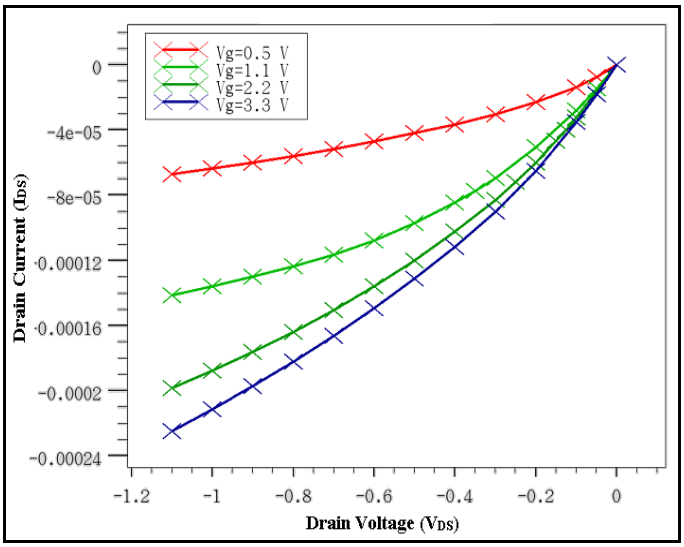

Figure 2: Graph of I_{DS}-V_{DS}

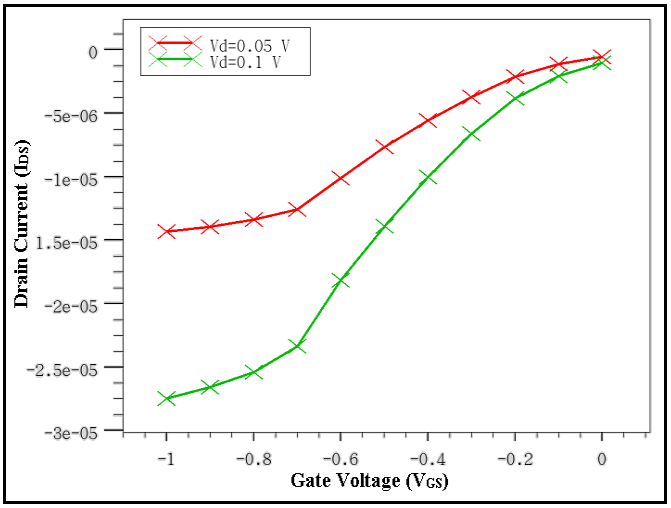

Figure 3: Graph of I_{DS}-V_{GS}

III. RESULTS AND DISCUSSION

36 simulations of L9 Orthogonal Array of Taguchi method were applied in this research to optimize the V_{TH} and I_{OFF} values using control factors that were listed in Table 2. In this research, V_{TH} belongs to nominal-the-best quality characteristic while I_{OFF} belongs to lower-the-best quality characteristic. The initial results of V_{TH} and I_{OFF} were listed in Table 4 and Table 5 respectively.

Table 4
V_{TH} Results for p-Type Transistor

Exp. No	Threshold voltage, V_{TH} (V)			
	X_1Y_1	X_1Y_2	X_2Y_1	X_2Y_2
1	0.24358	0.243365	0.24315	0.242937
2	0.237851	0.237633	0.237386	0.237168
3	0.231531	0.231313	0.23103	0.230812
4	0.250575	0.250366	0.250189	0.249976
5	0.233934	0.233719	0.233523	0.23331
6	0.262981	0.26277	0.262545	0.262332
7	0.244912	0.2447	0.244515	0.244302
8	0.274721	0.274513	0.274348	0.274136
9	0.258453	0.258243	0.258061	0.257852

Table 5
IOFF Results for p-Type Transistor

Exp. No	Leakage Current, I_{OFF} (nA/um)			
	X_1Y_1	X_1Y_2	X_2Y_1	X_2Y_2
1	52.217	52.422	52.6363	52.8428
2	58.3183	58.5485	58.8322	59.0647
3	65.9534	66.2154	66.5826	66.8475
4	45.2084	45.3838	45.5318	45.7087
5	65.0706	65.324	65.5665	65.8223
6	35.6784	35.818	35.9749	36.1159
7	52.3622	52.5649	52.7469	52.9514
8	52.217	52.422	52.6363	52.8428
9	58.3183	58.5485	58.8322	59.0647

Next, S/N Response and ANOVA were measured and laid out in Table 6 and Table 7 based on results in Table 4 and Table 5. Best parameters were then chosen based on highest contribution on S/N Response and ANOVA. The results of S/Response and ANOVA for V_{TH} and I_{OFF} both were shown in Table 6 and Table 7 respectively. From Table 6, it can be seen that Halo Implantation was set to be the dominant factor due to the highest influence on V_{TH} (52%). Adjustment factor was chosen based on the lowest possible variance value with the highest means which in this case is the Halo tilting angle. This parameter was swept between 19.7° to 19.9° to get V_{TH} to be closer to the nominal value. For I_{OFF} analysis which is shown in Table 7, Halo Implantation was also set as the dominant

factor due to the major effect (46%) on the variance. The recommended process parameters for V_{TH} and I_{OFF} are A_3, B $_{(swept)}$, C_3, D_3 and A_3, B_1, C_3, D_2 respectively where best setting parameters based on the Taguchi analysis was shown in Table 8.

The device was then simulated again using the best values laid out in Table 8 at different noise factor to verify the accuracy of Taguchi method. The results of V_{TH} and I_{OFF} at different noise factor were shown in Table 9. For simplicity, the average value of V_{TH} and I_{OFF} were measured and then compared to 2013 ITRS prediction. The final results of comparison between optimized, non-optimized and ITRS prediction were shown in Table 10.

Table 6
S/N Response and ANOVA for V_{TH}

Control Factor	S/N Ratio			Factor Effect (%)	
	Level 1	Level 2	Level 3	Variance	Means
A	56.74	57.62	58.05	52	56.23
B	58	57.46	56.96	32	40.56
C	57.29	57.47	57.65	4	3.01
D	57.14	57.51	57.77	12	0.19

Table 7
S/N Response and ANOVA for I_{OFF}

Control Factor	S/N Ratio			Factor Effect (%)
	Level 1	Level 2	Level 3	Variance
A	-15.58	-9.95	-1.32	46
B	-4.41	-10.66	-11.78	14
C	-16.56	-5.23	-5.06	38
D	-8.62	-7.6	-10.63	2

Table 8
Best Setting of Process Parameters

Control Factor	Unit	Best Value	
		V_{TH}	I_{OFF}
A	atom/cm^3	5.15 x 10^{13}	5.15 x 10^{13}
B	°	19.7	19.7
C	atom/cm^3	9.20 x 10^{12}	9.20 x 10^{12}
D	atom/cm^3	1.8 x 10^{11}	1.1 x 10^{11}

Table 9
Result of Confirmation Experiment

Parameter	X_1Y_1	X_1Y_2	X_2Y_1	X_2Y_2	Average
V_{TH} (V)	0.24892	0.24873	0.24856	0.24833	0.24864
I_{OFF} (pA/um)	5.23622	5.25649	5.27469	5.29514	5.26564

Table 10
Simulation Results vs. 2013 ITRS Prediction

Parameter	ITRS Prediction	Non-Optimized Results	Optimized Results
V_{TH}	-0.23 ± 12.7 % V	-0.211446V	-0.248635V
I_{OFF}	<100nA/um	100nA/um	5.26pA/um

IV. CONCLUSION

The statistical modelling of 14nm high-k metal gate p-type transistor was successfully reported. Silvaco TCAD Tools was used in this research as a tool of simulation while Taguchi method was applied for the optimization process. The result of optimum threshold voltage and low leakage current were reported to be well within the ITRS 2013 prediction and better than the results before optimization.

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