Statistical Modelling of 14nm N-Types MOSFET

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***Abstract*—This paper focuses on virtual modelling and optimization of 14nm n-types planar MOSFET. Here, high-k dielectric and metal gate were used where the high-k material is Hafnium Dioxide (HfO_2) and the metal gate is Tungsten Silicide (WSi_2). 36 simulations of Taguchi L9 Orthogonal Array method were applied in order to obtain the best parameter design for optimization of both performance parameters which are threshold voltage (V_{TH}) and leakage current (I_{OFF}). The simulation and fabrication for n-type transistor was conducted through Virtual Wafer Fabrication (VWF) Silvaco TCAD Tools named ATHENA and ATLAS for its electrical characterization. For analyzation of the impact parameters on V_{TH} and I_{OFF}, two noise parameters and four process parameters value were varied. From the simulations, the results show the best value were well within ITRS prediction where V_{TH} and I_{OFF} are 0.236737 V and 6.995705 nA/um respectively.**

***Index Terms*—14nm n-type MOSFET, High-k Dielectric, Silvaco TCAD Tools, Taguchi Method.**

I. INTRODUCTION

The 2013 ITRS roadmap proudly announces the continual scaling of CMOS for planar transistor because of the transistor scaling was actually at a critical interim and scaling in the sub-100nm regime seems impossible. This marvel gives a prodigious momentum to the IC industry and pushed the existing planar CMOS technology down to its physical limits at once. The problems are short channel effect (SCE) drain induced barrier lowering (DIBL), and hot carrier effect will give drawbacks to the system performance [1]. To solve the problem, an excellent device scheme should be made and major process barrier must be settling conclusively. Confronting this fundamental limit of transistor pushes the industry and research community to dynamically search for an alternative materials or new device architectures. Bin Yu et. al in [2] discusses and proposes on the major fabrication challenges, device scalability and performance which can be consider during the device fabrication process and design. The author also proved that the gate scaling up to 15nm is possible to implement and the performance is also tolerable enough.

In this paper, a planar high-k metal gate n-type transistor was optimized using L9 Orthogonal Array based on the 14nm design where the details can be seen in [3]. Briefly, the process in getting the right recipe for n- and p- type transistor design is simply through analysing their electrical characterization and load profile which is produced by ATLAS Simulator until the results of both threshold voltage (V_{TH}) and leakage current (I_{OFF}) are well within the 2013 ITRS prediction. For optimization process, the focus is mainly on two performance parameters which are the threshold voltage (V_{TH}) and leakage current (I_{OFF}) as it is the aim of the research to have a high performance with low leakage current device. For 36 simulations that we conducted will used two noise factors and four control factors. All these parameters are chosen based on Husam's suggestion in [4]. The control factor includes Halo Implantation dose (A), Halo Tilting Angle (B), S/D Implantation dose (C) and Compensation Implantation dose (D). Noise factor contains to factor of temperature that is Sacrificial Oxide Layer Temperature (X) and BPSG Temperature (Y). After completing the 36 simulations, a conclusion is then made based on the best result of the confirmation experiment and a corresponding topology where it depends on many factors closely related to the technology of implementation.

This paper was configured by the structure as follows: Section 2 explanation of the experiment designs of the transistor; Section 3 explanations about performance analysis and the results; and Section 4 conflations of the experiment.

II. EXPERIMENT DESCRIPTION

A. ATHENA Simulation Recipes

The experiment starts with virtually fabricating the n-type transistor using ATHENA module which is based on previous experiments by [5-8]. First of all was to initiate the silicon bulk at <100> orientations and then performed an oxide layer on the above layer by using dry oxygen at a temperature of 970°C for 20 minutes. For this stage boron was use as a dopant at a dose of $3.75x10^{12}$ions/cm^2. This is to orientate a mask for p-well implantation.

After that, in order to ensure the molecules of Boron isolated gently in the wafer, the silicon wafer was distributed in Nitrogen at a temperature of 900°C for 32 minutes and dry oxygen for 36 minutes. The masking oxide and distributed dry oxygen is etched consecutively at a temperature of 900°C for 25 minutes to produce pad oxide layer for Shallow Trench Isolator (STI). After that, low pressure chemical vapour

deposition process (LPCVD) was implemented and a 1500Å nitride layer and with a thickness of 1.0µm the photoresist deposition was deposited at the above of the oxide layer. After that the next process is to etch the photoresist and the nitride and move to the silicon bulk for trenching process. Then the trench wall passivation will distributed the surface at 900ºC.
Then proceed with a sacrificial oxide layer and sacrificial Nitride layer was grown and etched sequentially. It will cause the trench to be completed [9]. Two noise factors are introduced for Taguchi method application. The first process noise factor (X) is sacrificial oxide layer anneal temperature. The temperature was set at 900°C and 910°C for the device of fabrication process. Gate oxide was grown at temperature of 825°C by distributed the silicon bulk and dry oxygen. Next, a dosage of $1.75x10^{11}$ions/cm^2 boron difluoride (bf_2) was deposited in active area to modify the threshold voltage (V_{TH}) value at a temperature of 800 °C.

A 2nm thickness of HfO_2 and tungsten silicide (WSi_2) then stored sequentially in the bulk silicon and then etched consequently in order to obtain the desired gate contact point. These parameters were chosen based on paper in [10] which suggested HfO_2 as an insulator. It is because HfO_2 has high enough dielectric constant, band-gap and band-offset with silicon which will give low leakage and easier for scalability process. To get the best performance of n-type transistor, Halo implantation process was then implanted where indium was used as a dopant at a dose of $7.5535x10^{13}$ions/cm^2 with angle tilted at 32°. After that, nitride layer was deposited and etched in order to reveal the top of silicon layer and then formed the spacers for the both side of Poly-Si. Arsenic was implanted at a dose of $1x10^{14}$ions/cm^2, followed by Phosphor at a dose of $1.5x10^{12}$ions/cm^2 to achieve the great current value in the device.

A 0.5um Borophosphosilicate Glass (BPSG) was then deposited and annealed at temperature of 850°C for 20 minutes. The annealing temperature of Borophosphosilicate Glass (BPSG) was raised to 2°C to investigate the effect of process parameters on device performance. This process is a deviation from 850°C was the second factor for Noise Factor. This layer was performed for pre metal dielectric (PMD) [5]. The next step was to prepare the metal contact for source and drain by doping a $0.68x10^{14}$ ions/cm^2 of Phosphorous, annealed at a temperature of 850°C for 25 minutes and finally deposited an aluminium layer on the top of the structure and etched consequently to form the metal contact for source and drain.

The n-type transistor design was absolutely completed at this stage and proceeded with electrical characteristic simulation via ATLAS module. The results were then optimized with Taguchi's L9 orthogonal array which at this stage, 36 simulations were conducted using four parameters in order to discover the optimum threshold voltage and leakage current as per predicted in ITRS. The completed 14nm HfO_2/WSi_2 n-type transistor and its doping profile are as shown is Figure 1.

B. Taguchi Orthogonal L9 Array Method

In this simulation, the four factors set out by ATHENA was control different individually for process optimization. As a result, all parameters at each level can be properly simulated at different noise factors. From the explanation above, the four control factors that was used in this experiment includes Halo Implantation, Halo Tilt Angle, S/D Implantation and Compensation Implantation while the noise factors include Sacrificial Oxide Temperature and BPSG Temperature. The value of control factor and the noise factor was same in order to measure the V_{TH} and $I_{OFF.}$ This will allow the simulation neutral state which then makes it easier to facilitate results and strengthen the conclusion. All results of the control factors and noise factors at various levels have been listed in Table 1 and Table 2 respectively. The layout attempts to process L9 can be seen in [9].

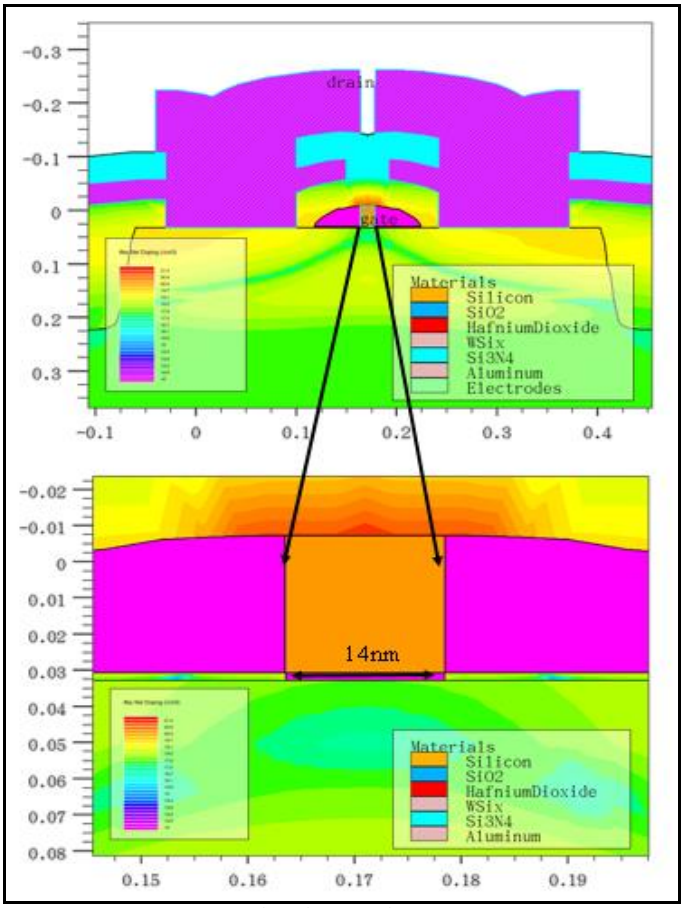

Figure 1: A Doping Profile of 14nm HfO_2/WSi_2 n-Type Transistor

Table 1
Control Factors and Their Levels

Symbol	Noise Factor	Unit	L1	L2
X	Sacrificial Oxide Temperature	°C	900	910
Y	BPSG Temperature	°C	850	852

Table 2
Noise Factors and Their Levels

Control Factor	Unit	L1	L2	L3
Halo Implant dose (A)	atom/cm^3	7.5530x10^{13}	7.5535x10^{13}	7.5540x10^{13}
Halo Tilt Angle (B)	°	31	32	33
S/D Implant dose (C)	atom/cm^3	0.99x10^{14}	1x10^{14}	1.1x10^{14}
Compensation Implant dose (D)	atom/cm^3	0.6751014	0.68x10^{14}	0.685x10^{14}

III. Performance Analysis And Results

A. ATLAS Overlay Results

The result for characteristic graphs which were produced through ATLAS can be seen in Figure 2 and Figure 3 respectively. The graph of drain current (I_{DS}) versus drain voltage (V_{DS}) at Vg=1.0 V, 1.5 V, 2.0 V and 2.5 V at the same time can be seen in Figure 2 while the graph of drain current (I_{DS}) versus gate voltage (V_{GS}) at Vd=0.5 V and 0.1 V at the same time can be seen in Figure 3. The results for I_{OFF} was extracted from the graph of subthreshold drain current (I_{DS}) versus gate voltage (V_{GS}). It is shown in Figure4. From the figure, the I_{OFF} value is 6.70457nA/um which is lower than the ITRS 2013 target.

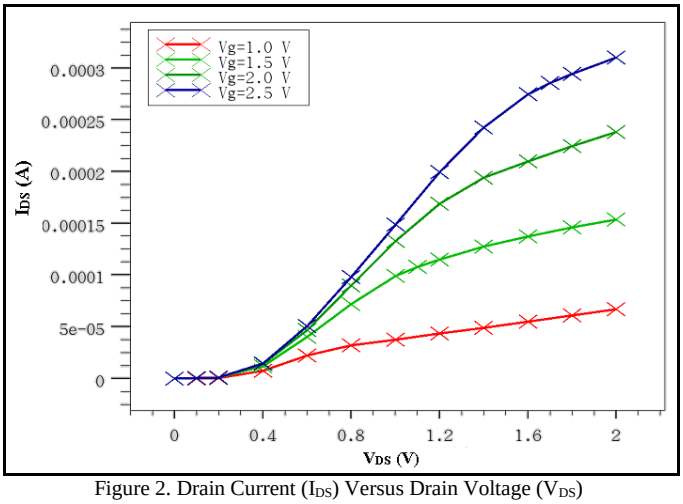

Figure 2. Drain Current (I_{DS}) Versus Drain Voltage (V_{DS})

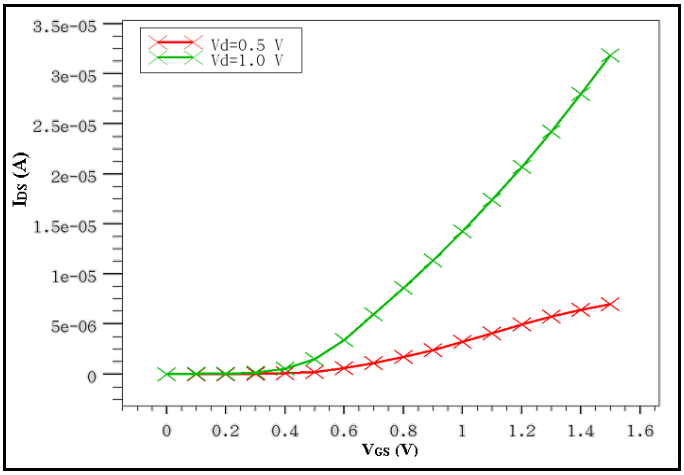

Figure 3. Drain Current (I_{DS}) versus Gate Voltage (V_{GS})

B. V_{TH} and I_{OFF} Optimization

In the optimization process, the device was simulated at three different levels of control factors with two noise factors where the steps of analysis already been discussed in [1, 4, 7]. In this experiment, V_{TH} is optimized using the nominal-the-best quality characteristic while I_{OFF} is optimized using the smaller-the-best quality characteristics. The simulation results of V_{TH} and I_{OFF} are as shown in Table 3 and Table 4 respectively.

To determine the characteristic quality of a process parameter of this experiment are from the factor impact percentage on S/N Ratio to reduce variation. The greater the S/N Ratio percentage indicates the higher influence of a process parameter on the device performance. Thus, the highest value of S/N Ratio at each process parameter is chosen to find the best combinations of the process parameters. The name of this process is analysis of variance (ANOVA). Table 5 shows the S/N Ratio response together with result of ANOVA analysis for V_{TH} and Table 6 shows the S/N Ratio response and ANOVA for I_{OFF}.

Table 3
V_{TH} Results for n-Type Transistor

Exp No.	Threshold Voltage, V_{TH} (V)			
	X1, Y1	X1, Y2	X2, Y1	X2, Y2
1	0.493733	0.485195	0.493934	0.4854
2	0.242297	0.230865	0.242553	0.231122
3	0.430243	0.438392	0.43003	0.438201
4	0.24858	0.239892	0.248834	0.240148
5	-0.16993	-0.169712	-0.169712	-0.178187
6	0.165606	0.156053	0.165873	0.156322
7	0.163056	0.171313	0.162839	0.171095
8	0.181527	0.172296	0.181792	0.172562
9	0.228356	0.219083	0.228613	0.219342

Table 4
I_{OFF} Results for n-Type Transistor

Exp No.	Leakage Current, I_{OFF} (nA/um)			
	X1, Y1	X1, Y2	X2, Y1	X2, Y2
1	5.10457	5.6501	5.09197	5.63618
2	70.55158	78.1233	70.3511	77.94
3	1599.7	16709.9	1597.93	1669.17
4	66.8282	72.3101	66.6709	72.1401
5	2029.08	2181.74	2025.23	2177.64
6	138.195	149.92	137.875	149.573
7	1912.97	2054.57	1909.31	2050.68
8	120.804	131.081	120.523	130.506
9	79.6634	86.5428	79.4766	86.3403

Table 5
S/N Response and Anova for V_{TH}

S	S/N Ratio (dB)			Factor Effect (%)	
	L1	L2	L3	Variance	Mean
A	29.91	21.56	29.65	40	46
B	24.55	29.98	26.6	13	29
C	29.64	29.38	22.1	32	18
D	30.39	25.02	25.72	15	7

Table 6
S/N Response and Anova for I_{OFF}

S	S/N Ratio (dB)			Factor Effect on Variance (%)
	L1	L2	L3	
A	137.57	131.17	131.22	1
B	140.87	131.37	124.72	11
C	146.74	142.45	107.77	79
D	140.18	131.15	125.53	9

From the results, it shows that factor A has a major effect on V_{TH} (40%), so it will be dominant factor. Since factor B give the lowest impact on S/N Ratio (13%) but highest on Mean (29%), thus it will take as the adjustment factor. Factor B is varies between 31° to 33° to get the V_{TH} near to nominal value. For I_{OFF}, factor C gives a major effect (79%) so it will set as a dominant factor. The best parameters that was declared by Taguchi method was shown in Table 7. To get the nominal value of V_{TH}, level 1 for Factor A, level 2 for Factor B, level 1 for Factor C and D were chosen. In order to get the lowest leakage, Taguchi Method suggested level 1 to be varies for all process parameters. Using the chosen value, the device was simulated again at different noise factor. It is to authorize the accuracy of Taguchi analysis prediction. The results of confirmation experiment were shown in Table 8.

In this research the mean value was taken as the final results for both performances. Finally, the simulation result was compared to the 2013 ITRS prediction and non-optimized results from [3] which was shown in Table 9. The results show an enormous device's performance compared to both ITRS prediction and non-optimized results as it produces a very low leakage current and the V_{TH} value was also within the ITRS prediction.

Table 7
Best Setting of Process Parameters

Process Parameter	Units	Best Value	
		V_{TH}	I_{OFF}
Halo Implantation	atom/cm3	$7.5530x10^{13}$	$7.5530x10^{13}$
Halo Tilt Angle	°	32	31
S/D Implantation	atom/cm3	$0.99x10^{14}$	$0.99x10^{14}$
Compensation Implantation	atom/cm3	$0.675x10^{14}$	$0.675x10^{14}$

Table 8
Results of Confirmation Experiment

Parameter	X1, Y1	X1, Y1	X1, Y1	X1, Y1	Mean
V_{TH} (V)	0.242397	0.230766	0.242653	0.231132	0.236737
I_{OFF} (nA/um)	6.70457	7.1501	6.89197	7.23618	6.995705

Table 9
Simulation Results vs. 2013 ITRS Prediction

Parameter	ITRS Prediction	Non-Optimized Results [3]	Optimized Results
V_{TH} (V)	0.23	0.232291	0.236737
I_{OFF} (nA/um)	<100	77.11	6.995705

IV. CONCLUSIONS

The 14nm high-k metal gate n-type device was successfully designed and presented. The optimization of threshold voltage (V_{TH}) and leakage current (I_{OFF}) using Taguchi L9 Orthogonal Array was also been fully utilized. The results are reported to be well within the 2013 ITRS prediction with leakage current below than the prediction 6.995705nA/um and V_{TH} of 0.236737V.

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REFERENCES

[1] H.A. Elgomathi, B. Yeop Majlis, F. Salehuddin, I. Ahmad, A, Zaharim, F.A. Hamid,"Optimizing 35nm NMOS Devices Vth and Ileak by Controlling Active Area and Halo Implantation Dosage," RSM2011 Proc., pp. 286-290, 2011.

[2] Bin Yu, Haihog Wang, Amol Joshi, et. al, "15nm Gate Length Planar CMOS Transistor," IEEE-IEDM, pp.937-939, 2001.

[3] Noor Faizah Z.A, I. Ahmad, P.J. Ker, et. al, "Modeling of 14 nm Gate Length n-Type MOSFET," IEEE-RSM Proc, 2015.

[4] H.A. Elgomati, B.Y. Majlis, A.M. Abdul Hamid, et. al., "Modelling of Process Parameters for 32nm PMOS Transistor Using Taguchi Method", Sixth Asia Modelling Symposium, 2012.

[5] Afifah Maheran A.H., Menon P.S., I. Ahmad, H.A. Elgomati, B.Y. Majlis, F. Salehuddin, "Scaling Down the 32 nm Gate Length NMOS Transistor to 22nm," IEEE-ICSE Proc.,pp. 191-194, 2012.

[6] Ibrahim Ahmad, Yeap Kim Ho, Burahanuddin Yeop Majlis, "Fabrication and Characterization of a 0.14 um CMOS device using ATHENA and ATLAS simulators," Semiconductor Physics, Quantum Electronic& Optoelectronics, vol. 9, pp. 40-44, 2006.

[7] H.A. Elgomathi, B. Yeop Majlis, F. Salehuddin, I. Ahmad, A, Zaharim, F.A. Hamid, "Optimizing 35nm NMOS Devices Vth and Ileak by Controlling Active Area and Halo Implantation Dosage," RSM2011 Proc., pp. 286-290, 2011.

[8] X. Chen, S. Samavedam, V. Narayanan, K. Stein, C. Hobbs, "A Cost Effective 32mn High-K/Metal Gate CMOS technology for Low Power Applications with Single-Metal/Gate-First Process," Symposium on VLSI Technology Digest of Technical Papers, pp. 88-89, 2008.

[9] Afifah Maheran A.H., Menon P.S., I.Ahmad , H.A.Elgomati, B.Y. Majlis, F.Salehuddin, "Design and Optimization of 22nm NMOS Transistor," Australian Journal of Basic and Applied Sciences, pp.1-8, 2012.

[10] Norani Bte Atan, Ibrahim Bin Ahmad, Burhanuddin Bin Yeop Majlis and Izzati Binti Ahmad Fauzi, "Effects of High-K Dielectric with Metal Gate for Electrical Characteristics of Nanostructured NMOS," International Conference on Engineering and ICT (ICEI 2014), pp.1-5, 2014.