Minimum Component, Electronically Tunable Simulator for Grounded Inductor with Low Parasitic Effects

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***Abstract*—A new grounded inductor simulator employing single voltage differencing trans-conductance amplifier (VDTA) and one grounded capacitor has been proposed. The proposed circuit requires minimum number of active and passive elements and offers several advantageous features, which are not simultaneously available with any of the previously reported grounded inductor simulator. The presented configuration provides the electronic tuning of simulated inductance by varying the biasing current of VDTA. Under the influence of VDTA port parasitic impedances, the proposed design offered better performance than the previously reported circuit with similar active and passive component requirements. Further, the high frequency limitation under the non-ideal conditions has been discussed. On non-ideal analysis, the realized circuit was found to be less sensitive as the sensitivity indexes were not more than unity in magnitude. To confirm the working of the proposed circuit as a grounded inductor simulator, it has been used to realize the second order band-pass filter. The performance of realized inductor simulator and band pass filter was demonstrated by SPICE simulations with TSMC CMOS .18µm process parameters.**

***Index Terms*—Electronic Control; Grounded Inductor; Inductor Simulator; VDTA.**

I. INTRODUCTION

An inductor in grounded form finds applications in several areas of analog signal processing/generation such as in filter design, sinusoidal oscillators, phase shifters and parasitic element cancellation. However, a conventional spiral inductor has several drawbacks, such as it has large size and weight, generates unwanted harmonics of the signals due to saturation of its core, picks as well as radiates electromagnetic waves etc. Its quality factor and liner dimensions are directly proportional to each other. Hence, it is not possible to design a small size inductor with high quality factor. Thus, the active simulation of grounded inductors has become a popular research area, in which a grounded inductor is realized by using active building blocks (ABBs) and external capacitors and resistors. Numerous grounded inductor simulator circuits employing different ABBs such as operational amplifiers (Op-amp) [1]-[4], [6], [9], current conveyors (CC) [5], [8],[10]-[16], differential voltage current conveyors (DVCC) [7], current feedback operational amplifiers (CFOA) [17]-[19], [26], current differencing trans-conductance amplifiers (CDTA)[20], four terminal floating nullors (FTFN) [21], current follower trans-conductance amplifiers (CFTA) [22], fully differential second generation current conveyors (FDCCII)[23], voltage differencing differential input buffered amplifiers (VDDIBA) [24], differential difference current conveyors (DDCC) [25,29], dual-x second generation current conveyors (DX-CCII) [27,28], operational trans-resistance amplifiers (OTRA) [30], voltage differential buffered amplifiers (VDBA) [31] and voltage differencing trans-conductance amplifiers (VDTA) [32] have been proposed in the literature, but unfortunately all of the reported circuits suffer from one or more of the following drawbacks: (i) use of more than one ABB, (ii) use of external resistor(s), (iii) use of floating capacitor, (iv) lack of electronic controllability (v) requirement of component matching (vi) degraded non ideal performance and (v) high parasitic effects.

Therefore, the purpose of this communication is to propose a new grounded inductor simulator circuit with the following advantageous features; (i) use of single VDTA, (ii) no use of any external resistor, (iii) use of grounded capacitor, (iii) availability of electronic control of inductance, (iv) no requirement of any component matching constraint, (v) good non-ideal performance and (vi) reduced parasitic effects.

II. PROPOSED CONFIGURATION

VDTA is a versatile active element [33] found in several applications in analog signal generation and processing [35-41]. Symbolic representation and CMOS implementation of conventional VDTA [34] are shown in Figure 1 and Figure 2 respectively, where "V_P" and "V_n" are input terminals and "Z", "X^+" and "X^-" are output terminals. All terminals of VDTA exhibit high input impedance values. The terminal characteristics of VDTA can be described by:

$$\begin{bmatrix} I_Z \\ I_{X^+} \\ I_{X^-} \end{bmatrix} = \begin{bmatrix} g_{m_1} & -g_{m_1} & 0 \\ 0 & 0 & g_{m_2} \\ 0 & 0 & -g_{m_2} \end{bmatrix} \begin{bmatrix} V_{V_P} \\ V_{V_N} \\ V_Z \end{bmatrix} \quad (1)$$

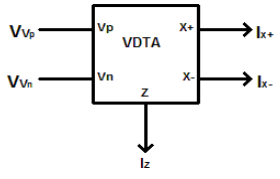

Figure1: The symbolic representation of VDTA

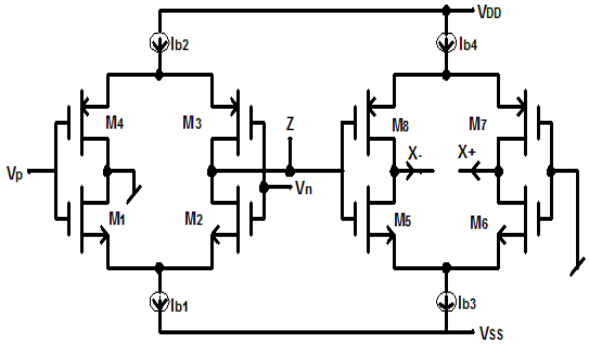

Figure 2: The CMOS realization of VDTA [34]

The trans-conductance gains g_{m1} and g_{m2} of CMOS VDTA shown in Figure 2 are given by Equation (2) and (3).

$$g_{m_1} = \frac{g_3 + g_4}{2} \tag{2}$$

$$g_{m_2} = \frac{g_5 + g_8}{2} \text{ or } g_{m_2} = \frac{g_6 + g_7}{2} \tag{3}$$

where, g_n is the trans-conductance of n^{th} MOS transistor given in Equation (4).

$$g_n = \sqrt{I_{B_n} \mu_n C_{OX} \left(\frac{W}{L}\right)_n} \tag{4}$$

In Equation (4), μ_n is carrier mobility, C_{OX} is capacitance of gate-oxide layer per unit area, W is MOS transistor's effective channel width, L is effective channel length and I_{Bn} is bias current of n^{th} transistor

The proposed grounded inductor simulator configuration is shown in Figure 3.

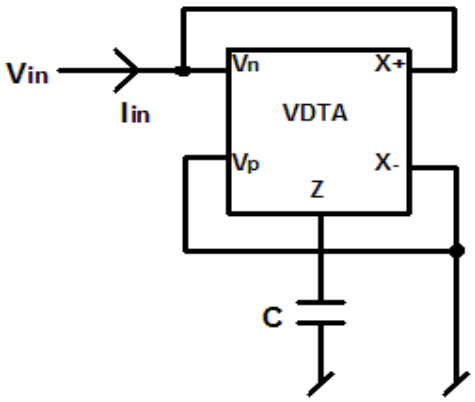

Figure 3: Proposed grounded inductor simulator configuration

A routine analysis of this circuit yields the following expression for its input impedance:

$$Z_{in} = \frac{sC}{g_{m_1} g_{m_2}} \tag{5}$$

which simulates a grounded inductor of inductance value:

$$L_{eq} = \frac{C}{g_{m_1} g_{m_2}} \tag{6}$$

Thus, the inductance value of simulated inductor can be electronically controlled by trans-conductance g_{m1} or g_{m2}. The values of g_{m1} and g_{m2} can be changed by bias currents of VDTA.

III. Non-Ideal Analysis

Under the influence of non-idealities, the terminal relationships of VDTA are modified as;

$$\begin{bmatrix} I_Z \\ I_{X^+} \\ I_{X^-} \end{bmatrix} = \begin{bmatrix} \beta_z g_{m_1} & -\beta_z g_{m_1} & 0 \\ 0 & 0 & \beta_{x+} g_{m_2} \\ 0 & 0 & -\beta_{x-} g_{m_2} \end{bmatrix} \begin{bmatrix} V_{V_P} \\ V_{V_N} \\ V_Z \end{bmatrix} \tag{7}$$

where β_z, β_{x+}, β_{x-} are transconductance error gains of VDTA.

The input impedance of presented configuration under non-ideal conditions is found as:

$$Z_{in} = \frac{sC}{\beta_z \beta_{x+} g_{m_1} g_{m_2}} \tag{8}$$

which model a lossless grounded inductor with inductance value;

$$L_{eq} = \frac{C}{\beta_z \beta_{x+} g_{m_1} g_{m_2}} \tag{9}$$

Hence, it can be seen from (9) that even under the non-ideal conditions, the proposed circuit simulated a grounded inductor without any loss term associated with it. The factor $1/\beta_z\beta_{x+}$ is a multiplication factor with a value just above the unity as the typical values of β_z and β_{x+}, which are very slightly less than unity (around .995). Thus, the behavior of proposed circuit is not diverted by VDTA non-idealities.

The sensitivity figures of inductance of simulated grounded inductor with respect to capacitor/ transconductance gains/ gain errors are found as:

$$-S_C^{L_{eq}} = S_{g_{m1}}^{L_{eq}} = S_{g_{m2}}^{L_{eq}} = S_{\beta_z}^{L_{eq}} = S_{\beta_{x+}}^{L_{eq}} = -1 \tag{10}$$

So, all the sensitivities of L_{eq} are low and not more than unity in magnitude.

IV. Effects of Parasitics

The performance of the proposed grounded inductor was also investigated under the influence of VDTA port parasitics. X+ port parasitic impedance consists of a capacitor C_{x+} in parallel with resistance R_{x+}, while X- port parasitic impedance consists of a capacitor C_{x-} in parallel with resistance R_{x-}. Further, Vp port parasitic impedance consists of a capacitor C_P in parallel with resistance R_P, and Vn port parasitic impedance consists of a capacitor C_N in parallel with resistance R_N and Z port parasitic impedance

consists of a capacitor C_Z in parallel with resistance R_Z. The input impedance of proposed configuration considering the VDTA port parasitics is found to be:

$$Z_{in} = \frac{\left(\frac{1}{R_Z} + sC + sC_Z\right)}{(g_{m_1} g_{m_2}) + \left(\frac{1}{R_Z} + sC + sC_Z\right)\left(\frac{1}{R_{x+}} + \frac{1}{R_N} + sC_{x+} + sC_N\right)} \quad (11)$$

The equivalent circuit derived from Equation (11) is shown in Figure 4.

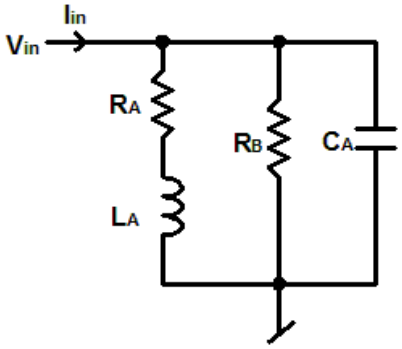

Figure 4: Equivalent circuit of proposed configuration under the influence of VDTA port parasitics

where:

$$R_A = \frac{(1/R_Z)}{g_{m_1} g_{m_2}} \quad (12)$$

$$R_B = \frac{1}{(1/R_{x+} + 1/R_N)} \quad (13)$$

$$L_A = \frac{(C + C_Z)}{g_{m_1} g_{m_2}} \quad (14)$$

$$C_A = (C_{x+} + C_N) \quad (15)$$

Now, it can be illustrated from Figure 4 that L_A is intended grounded inductance while R_A, R_B and C_A are lossy terms. So, due to VDTA port parasitics, the pure inductor simulator becomes a lossy simulator with several lossy terms.

The parasitics impedances available at port "V_P" and "X-" were not effective as these ports were grounded. The effect of parasitic capacitance "C_z" can be eliminated by adding it with external capacitance "C". The parasitics resistance "R_z" available at "Z" port and parasicis impedances available at port "X+" and "V_n" were not balanced by any external element, so these parasitic impedances became significant in high frequency region and effect the performance of proposed circuit. So, the maximum usable frequency (f_o) of presented circuit can be found as:

$$f_{0_{\max}} \langle\langle \min\left\{\frac{1}{2\pi R_Z (C_Z + C)}, \frac{(\frac{1}{R_n} + \frac{1}{R_{x+}})}{2\pi (C_n + C_{x+})}\right\} \quad (16)$$

There is another grounded inductor simulator that employs a single VDTA and a single grounded capacitor proposed in [32], which is shown in Figure 5.

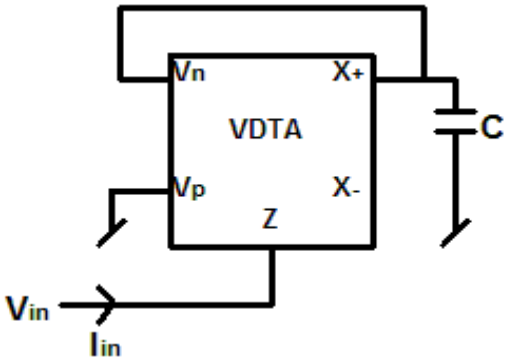

Figure 5: Grounded inductor simulator proposed in [32]

The input impedance and equivalent circuit of this configuration under the influence of VDTA parasitics are given by:

$$Z_{in} = \frac{\left\{s(C + C_{x+}) + \frac{1}{R_{x+}}\right\}}{\left\{s^2 C_Z (C + C_{x+}) + s\left\{\frac{(C + C_{x+})}{R_z} + \frac{C_z}{R_{x+}}\right\} + \frac{1}{R_{x+} R_z} + g_{m_1} g_{m_2}\right\}} \quad (17)$$

and:

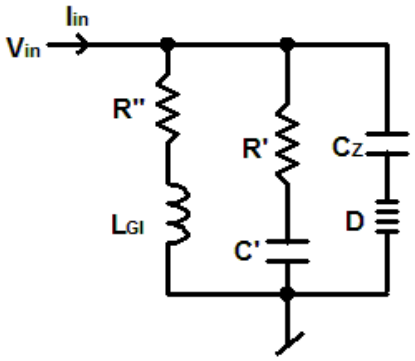

Figure 6: Equivalent circuit of grounded inductor simulator proposed in [32] under the effects of VDTA port parasitics

where:

$$L_{GI} = \frac{(C + C_{x+}) R_{x+} R_z}{(1 + g_{m_1} g_{m_2} R_{x+} R_z)} \quad (18)$$

$$R' = \frac{(C + C_{x+}) R_{x+} R_z}{R_{x+}(C + C_{x+}) + R_z C_z} \quad (19)$$

$$C' = \frac{(C + C_{x+}) R_{x+} + C_z R_z}{R_z} \quad (20)$$

$$R'' = \frac{R_z}{(1 + g_{m_1} g_{m_2} R_{x+} R_z)} \quad (21)$$

$$D = (C + C_{x+}) R_{x+} R_z \quad (22)$$

Now, it is clear from Figure 6, that L_{GI} is the intended grounded inductance while R', C', R'', C_z and D are the lossy terms. When compared Figure 4 with Figure 6, we found that the circuit shown in Figure 6 has more number of lossy terms as compared to circuit shown in Figure 4. Moreover, in Figure 4 only lossy capacitor C_A influences the frequency

response significantly as lossy resistors R_A and R_B do not have any external/parasitic capacitance terms in their expressions. On the other hand, with reference to the circuit as shown in Figure 6, all the lossy terms except R'' influence the frequency response significantly as external/parasitic capacitance terms available in their expressions. Thus, under the influence of VDTA port parasitics, the configuration proposed in [32] has large number of frequency dependent lossy terms, which disturbs the frequency response more. Hence, the proposed circuit has low parasitic effects than circuit proposed in [32] due to its improved circuit structure although both the circuits have same active and passive component requirements.

V. Application Example

The working of proposed grounded inductor simulator has been validated by using it in the realization of a second order band pass filter (BPF). The passive realization of simple RC second order low-pass is shown in Figure 7 and the active implementation of this filter employing the proposed grounded inductor simulator is illustrated in Figure 8.

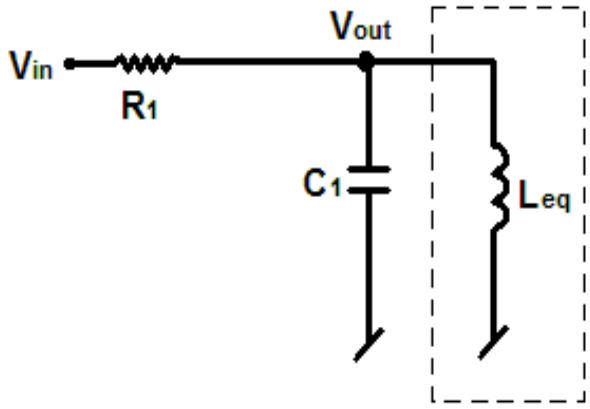

Figure 7: Passive RLC realization of voltage mode second order BPF

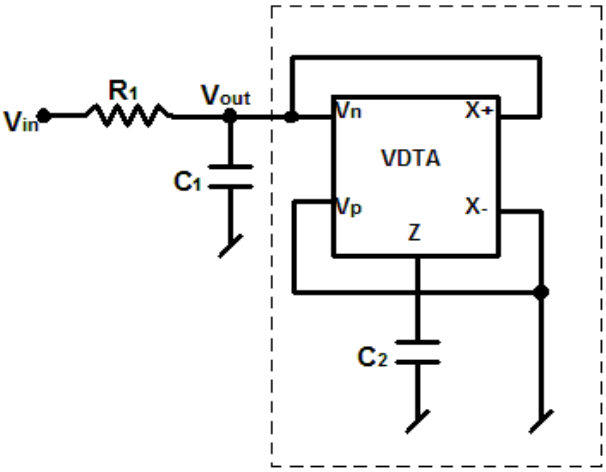

Figure 8: Active Realization of voltage mode second order BPF employing proposed grounded inductor simulator

The voltage transfer function of the realized filter of Figure 8 is given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{s\left(\frac{1}{R_1C_1}\right)}{s^2 + s\left(\frac{1}{R_1C_1}\right) + \frac{g_{m_1}g_{m_2}}{C_1C_2}} \quad (23)$$

The bandwidth (BW) and angular frequency (ω_0) obtained from Equation (23) are:

$$BW = \frac{1}{R_1C_1} \quad (24)$$

$$\omega_0 = \sqrt{\frac{g_{m_1}g_{m_2}}{C_1C_2}} \quad (25)$$

So, from Equation (24) and (25), it was found that BW and ω_0 of this band pass filter are independently controllable i.e. the BW by R_1 and ω_0 by g_{m1} or g_{m2} or C_2.

VI. Simulation Results

The performance of the proposed structure has been confirmed by SPICE simulations with CMOS VDTA [34]. The component values used were; C = 0.01nF, g_{m1} = g_{m2}= 636.3 µA/V and power supply ± 0.9V DC.

The magnitude response and the phase response of the proposed simulated inductor and simulator proposed in [32] are shown in Figure 9 and Figure 10 respectively. From Figure 9, it is clear that the simulated magnitude response of proposed inductor is same as the ideal magnitude response in the frequency range of 398 kHz to 31.62 MHz. Similarly, Figure 10 indicates that the ideal and simulated phase responses is almost identical in the frequency range of 3.12 MHz to 30.23 MHz. The deviation of simulated responses from ideal is due to non-ideal and parasitic effects.

When comparing the magnitude and phase response of our circuit and responses of circuit given in [32] with ideal response, it is clear from Figure 9 and 10 that at high frequencies, the magnitude and phase responses of circuit given in [32] is highly deviated from ideal response due to presence of high parasitic effects.

Our proposed circuit gave a better response at high frequencies due to low parasitic effects. Therefore, it is verified that proposed circuit experience less parasitic effects in comparison to the circuit given in [32].

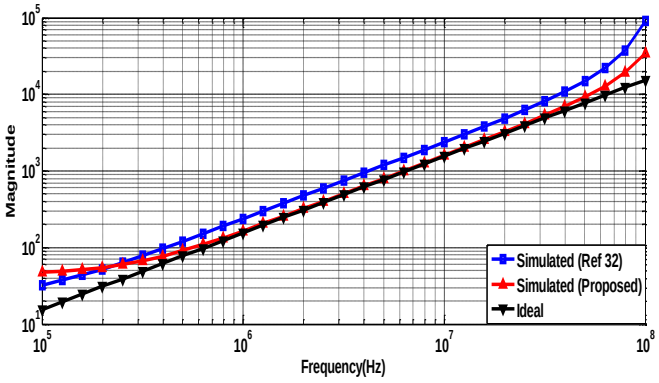

Figure 9: Magnitude response of proposed grounded inductor simulator with ideal response and response of circuit proposed in [32]

To confirm the validity of band-pass filter shown in Figure 7(b), it was simulated using the CMOS VDTA [34]

with R_1 = 1.58kΩ, C_1 = 5pF, C_2 = 0.01nF, g_{m1} = g_{m2}= 636.3 µA/V with power supply ± 0.9V DC. The frequency response of this realized band-pass filter is shown in Figure 11.

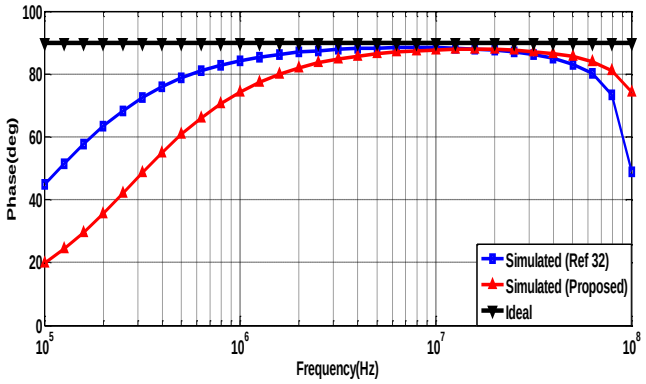

Figure 10: Phase response of proposed grounded inductor simulator with ideal response and response of circuit proposed in [32]

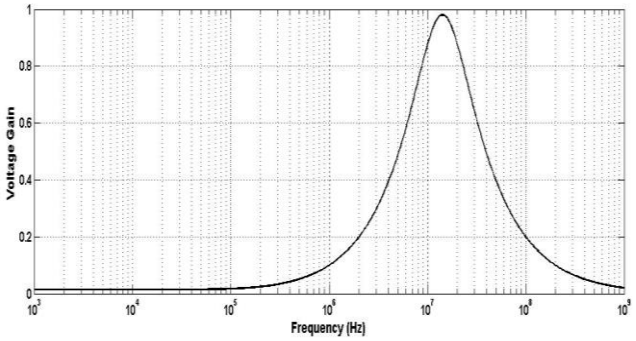

Figure 11: Frequency response of BPF given in Figure8

From Equation (4), it is clear that trans-conductance can be changed by changing the bias current. Thus, to demonstrate the electronic control of proposed configuration, magnitude responses have been plotted for different values of bias current I_b, where I_b= I_{b1}= I_{b2}= I_{b3}= I_{b4}. Figure 12 shows the magnitude responses at I_b= 150 µA, 160 µA, 170 µA and 180 µA.

The comparison of the proposed circuit with the previous reported grounded inductor simulators employing different ABBs has been given in Table 1.

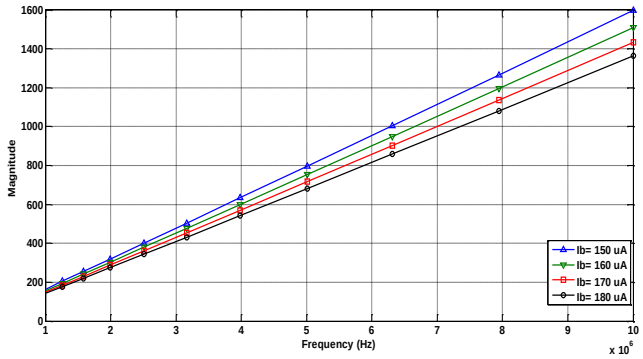

Figure 12: Magnitude responses of proposed grounded inductor at different values of bias currents

Table 1
Comparison of Proposed Grounded Inductor Simulators Circuit with Previously Proposed Grounded Inductor Simulator Circuit

Reference	Number of active elements	Number of Resistors	Number of capacitors	Requirement of component matching condition	Electronically tunable inductance
[1]	2	3-F	1-F	YES	NO
[2]	1	2-F+1-G	1-F	YES	NO
[3]	1	4-F+2-G	1-F	YES	NO
[5]	1	1-G+2-F	1-G	NO	NO
[6]	2	1-G+1-F	1-F	NO	NO
[7]	2	0	1-F	NO	YES
[8]	1	2-G+2-F	1-F	YES	NO
[9]	2	1-G+1-F	1-G	NO	NO
[10]	1	2-G+1-F	1-F	YES	NO
[11]	1	1-G+1-F	1-F	YES	NO
[12]	2	0	1-G	NO	YES
[13]	1	1-G+1-F	1-F	YES	NO
[14]	2	0	1-G	NO	NO
[15]	3	2-G+1-F	1-G	NO	NO
[16]	3	3-G+1-F	1-G	NO	NO
[17]	1	1-G+1-F	1-G	NO	NO
[18]	2	1-G+1-F	1-G	NO	NO
[19]	1	1-G	1-F	NO	NO
[20]	2	0	1-G	NO	YES
[21]	1	2-G+2-F	1-F	YES	NO
[22]	2	0	1-G	NO	YES
[23]	1	2-G	1-G	NO	NO
[24]	2	0	1-G	NO	YES
[25]	1	1-G+1-F	1-G1	NO	NO
[26]	1	1-G+1-F	1-F	NO	NO
[27]	1	1-G+1-F/ 1-G+2-F/ 3-G	1-F	YES	NO
[28]	1	2-G/3-G	1-F	NO	NO
[29]	1	1-G+1-F	1-G	YES	NO
[30]	2	2-F	2-F	YES	NO
[31]	1	1-F	1-F	NO	YES
[32]	1	0	1-G	NO	YES
Proposed	**1**	**0**	**1-G**	**NO**	**YES**

G* Grounded F* Floating

VII. CONCLUSION

A new lossless grounded inductor simulator employing one VDTA and single grounded capacitor has been proposed. The single ABB-based realizations has advantageous features, such as small chip area and low power dissipation, and the use of capacitor in grounded form is favorable from the monolithic integration point of view. The proposed configuration offers electronic controllability, no component matching constraint, good non-ideal performance, low active/passive sensitivities and reduced parasitic effects. The behavior of simulated grounded inductor has a close match with ideal behavior for a decade of frequency. The electronic tuning capability is confirmed by varying biasing currents. In future, some new VDTA based grounded inductors can be designed with wide operating frequency ranges using the proposed configuration. The workability of the proposed circuit has been confirmed by a design example of second order voltage mode band-pass filter. SPICE simulations have been performed to confirm the theoretical analysis.

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